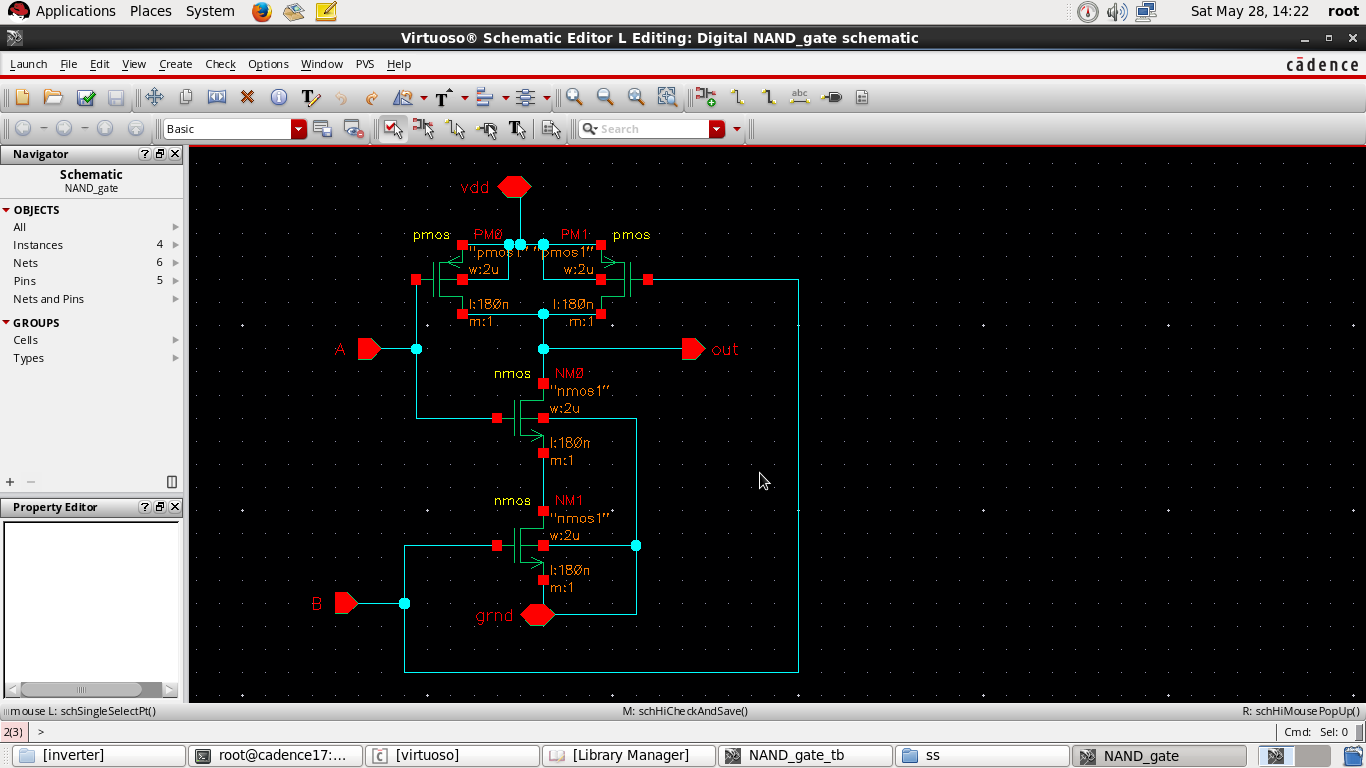
**Nand gate design using cadence**

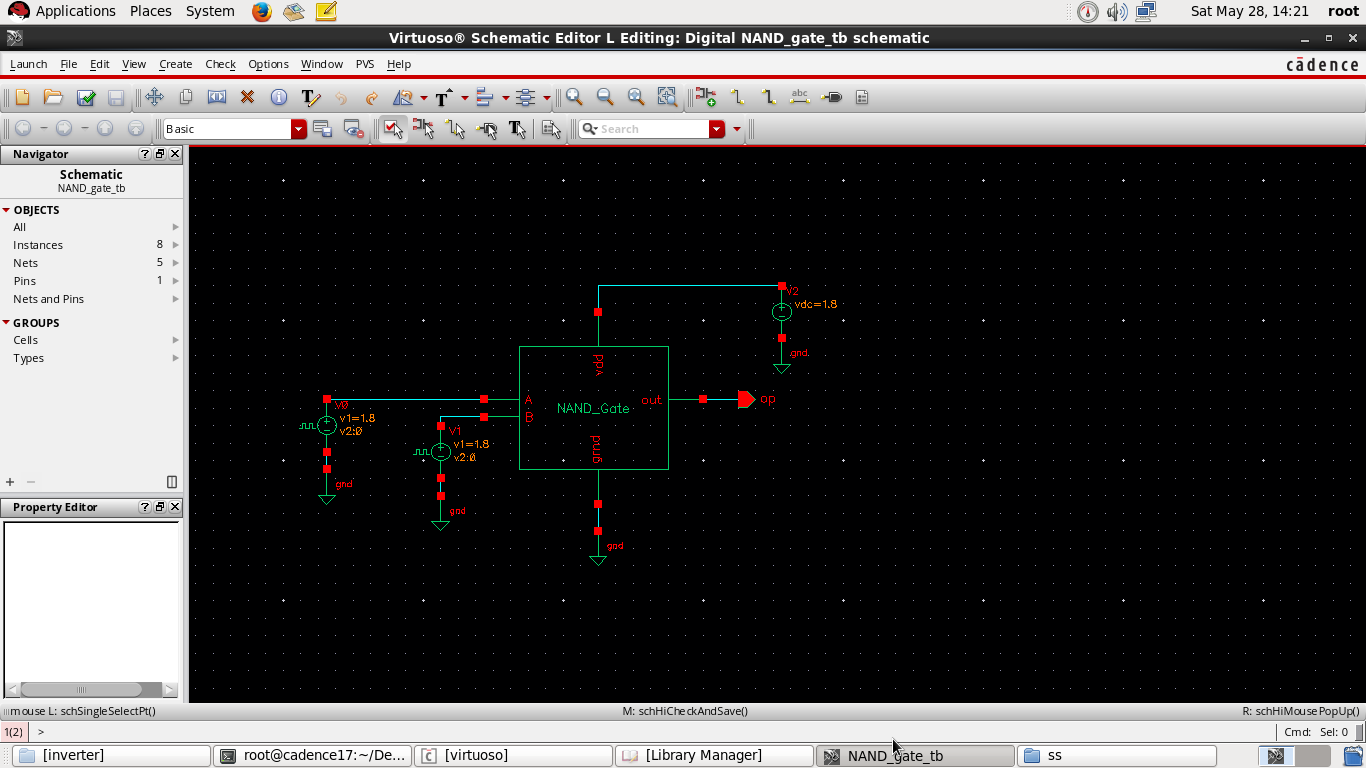
**Submitted by,**

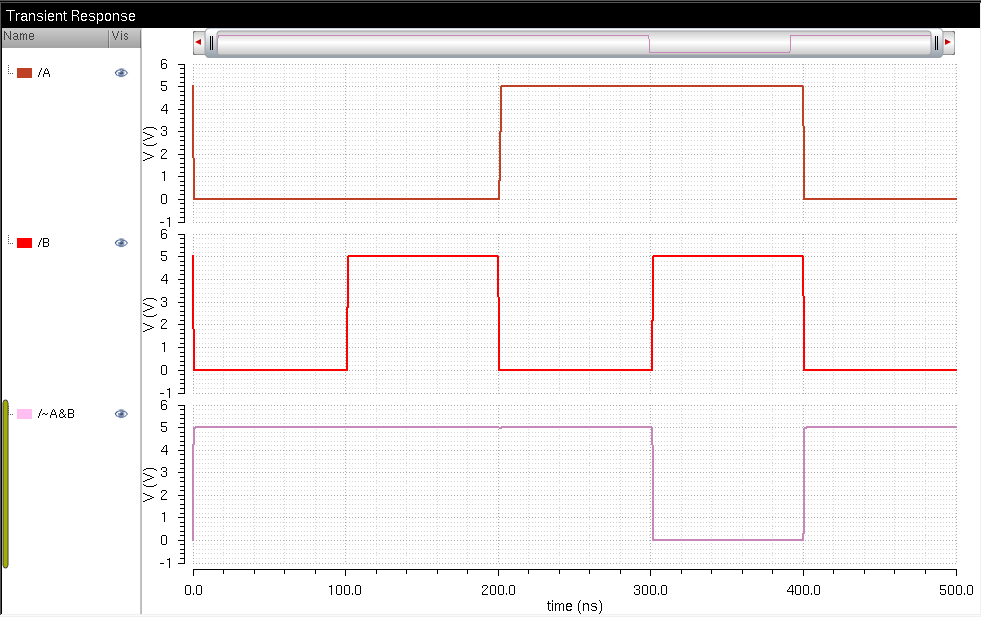
**Manoj M (20bec037)**

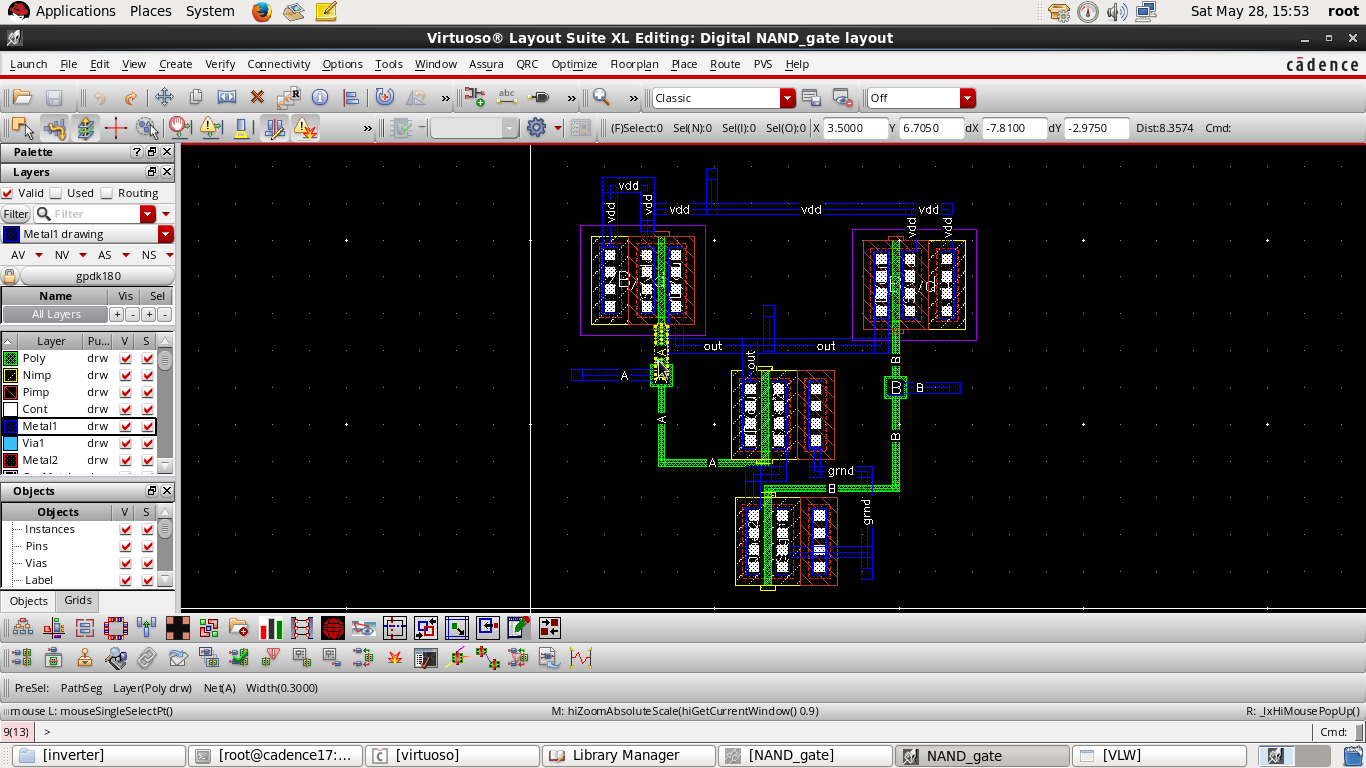
**Jai Prasanth C (21bec330)**

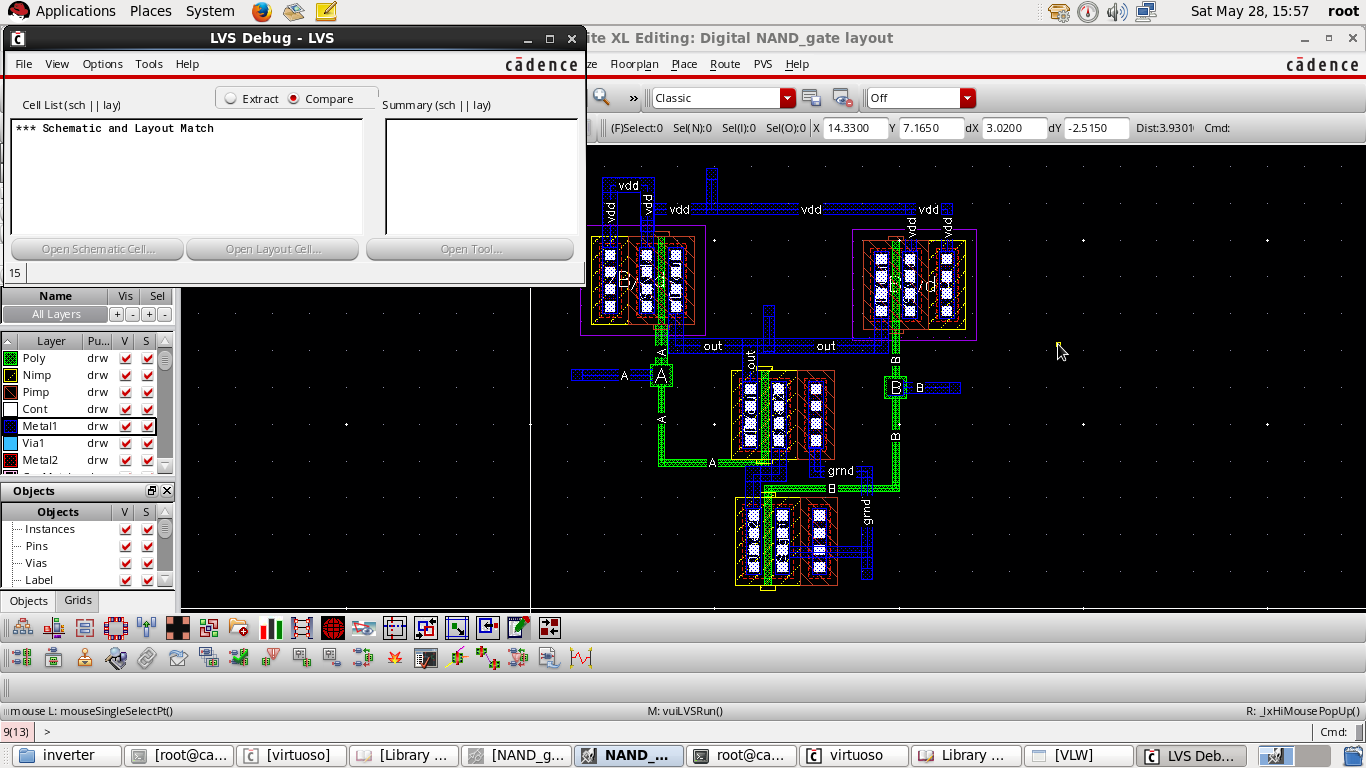
**Tegeshwaran G P (20bec061)**

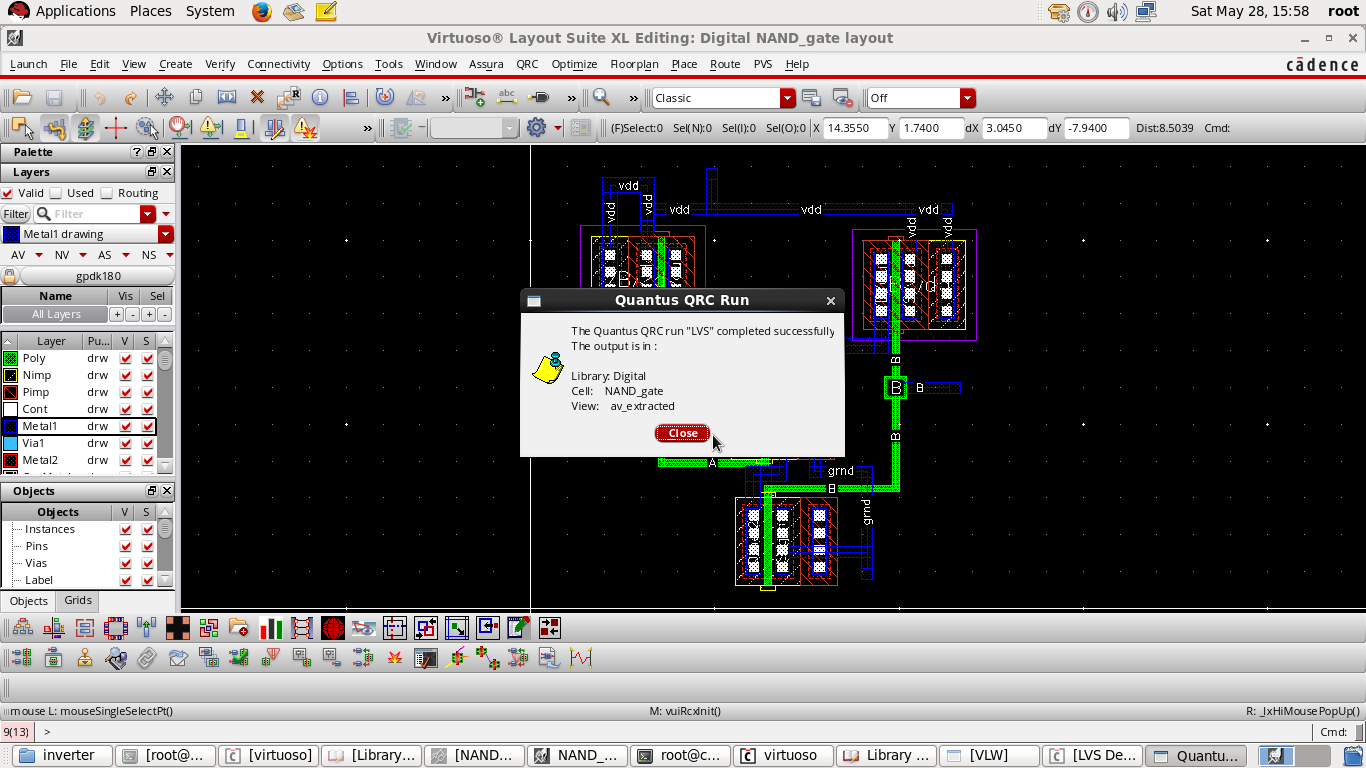
**Schematic:**

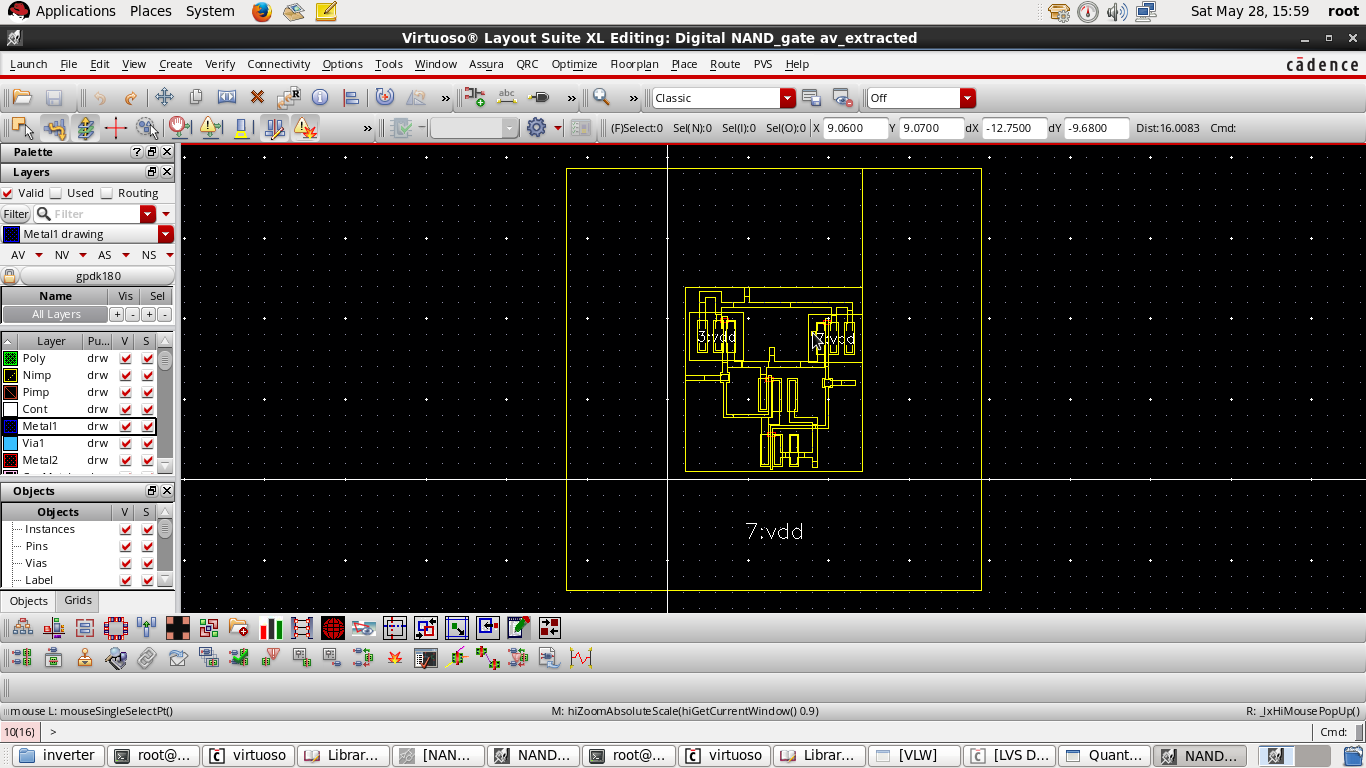
Symbol:

Simulation:

Layout:

Layout vs Schematic(LVS):

QRC:

Resistance capacitance extraction result: